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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/685,176	10/14/2003	Chandrasekaran N. Gupta	X-1532 US	4244

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EXAMINER	
ZHENG, EVA Y	
ART UNIT	**PAPER NUMBER**
2611	

DATE MAILED: 12/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

Office Action Summary	**Application No.** 10/685,176	**Applicant(s)** GUPTA ET AL.
	Examiner Eva Yi Zheng	**Art Unit** 2611

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *14-32* is/are allowed.

6)☒ Claim(s) *1-3 and 10-13* is/are rejected.

7)☒ Claim(s) *4-9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10/14/03* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). In paragraph [0021] of specification, "interface 110 is conventional". Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

2. Claim 2 is objected to because of the following informalities: on line 2, please add – of data – after "timed transfers" for claim clarification.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States

only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1, 2, 11 and 12 are rejected under 35 U.S.C. 102(e) as being unpatentable by To et al (US 6,941,484).

a) Regarding to claim 1, To et al disclose a data communication system, comprising:

a first integrated circuit (304 in Fig 3); and

a second integrated circuit coupled for source synchronous communication with the first integrated circuit (302 in Fig. 3);

the second integrated circuit including a recapture circuit (306), the recapture circuit configured to perform internally timed transfers of data (data transferred from block 304), the data obtainable from the first integrated circuit in association with a source clock domain (write clock), the internally timed transfers of the data being from the source clock domain into an internal clock domain of the second integrated circuit (as shown in Fig. 3).

b) Regarding to claim 2, To et al disclose the system, according to claim 1, wherein the internally timed transfers are responsive to a timing signal of the source clock domain from the first integrated circuit and an internal clock signal of the internal clock domain of the second integrated circuit (as shown in Fig. 3).

c) Regarding to claim 10, To et al disclose the system, according to claim 1, wherein the second integrated circuit comprises a digital clock module (inherent as 406 in Fig. 4), the digital clock module coupled to receive a clock signal of the internal clock domain and configured to provide a plurality of clock signals, the plurality of clock signals being phases of the clock signal (410 in Fig. 4 and Col 3, L66-Col 4, L23).

d) Regarding to claim 11, To et al disclose the system, according to claim 10, the clock signal are at 0, 90, 180, and 270 degrees to provide the plurality of clock signals (as shown in Fig. 7; Col 5, L1-10).

d) Regarding to claim 12, To et al disclose the system, according to claim 1, wherein at least one of the first and second integrated circuits comprises a programmable logic device (Col 8, L19-31).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 3 and 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over To et al (US 6,941,484) in view of Ehmann (US 6,701,390).

a) Regarding to claim 3, To et al disclose all the subject matters above except for the specific teaching of the recapture circuit.

However, Ehmann disclose a first data registration stage configured to capture the data in the source clock domain (read pointer 100 in Fig. 3);

a data valid signal generator configured to provide a valid data signal responsive to the internal clock signal and a derived signal from the timing signal (control logic 92 in Fig. 3); and

a second data registration stage configured to recapture the data in the internal clock domain responsive to the data valid signal and the internal clock signal (96 in Fig 3).

Both To et al and Ehmann are direct to clock synchronization in IC devices. Therefore, it is obvious to one of ordinary skill in art to implement the teaching of registration stages and valid signal generator of Ehmann in the memory controller teaching of To et al. By doing so, increase data bandwidth in IC transfers and optimize data and clock synchronization.

b) Regarding to claim 13, To et al disclose all the subject matters above except for the specific teaching of a plurality of FIFO buffers.

However, Ehmann, in the same field of endeavor disclose a bi-directional IC device comprise FIFO buffers under the logic control (enable signal) (Fig. 1-3). Both To et al and Ehmann are direct to clock synchronization in IC devices. Therefore, it is obvious to one of ordinary skill in art to implement the teaching of FIFO buffers of Ehmann in the memory controller teaching of To et al. By doing so, increase data bandwidth in IC transfers and optimize data and clock synchronization.

Allowable Subject Matter

7. Claims 4-9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. Claims 14-31 are allowed.

9. The following is an examiner's statement of reasons for allowance:

None of the prior art teaches or suggests an IC device comprise a recapture circuit, comprising a first plurality of registers, the first plurality of registers coupled to receive a data signal and a timing signal and configured to capture data into a clock domain of the timing signal; a frequency divider coupled to receive the timing signal and configured to provide an enable signal, the enable signal having a frequency less than the frequency of the timing signal; the first plurality of registers coupled to receive the enable signal; the first plurality of registers configured to provide a plurality of data phases, each of the data phases active on one of a leading edge or a lagging edge of the timing signal and one of high state or low state of the enable signal; a second plurality of registers, an input portion of the second plurality of registers coupled to receive the enable signal and an internal clock signal and configured to clock off of different edges of the internal clock signal, an output portion of the second plurality of registers coupled in series to the input portion and configured to clock off of different edges of the internal clock signal different from the input portion clockage; a logical operator coupled to receive output from the second plurality of registers and configured to provide a data valid signal therefrom; and a third plurality of registers, the third plurality of registers clocked responsive to the internal clock signal and write enabled responsive to the data valid signal, the third plurality of registers coupled to the first plurality of registers to receive output data therefrom and configured to recapture the output data into a clock domain of the internal clock signal.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eva Y Zheng whose telephone number is 571-272-3049. The examiner can normally be reached on M-F, 7:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on 571-272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Eva Yi Zheng
Examiner
Art Unit 2611

November 29, 2006

CHIEH M. FAN
SUPERVISORY PATENT EXAMINER